

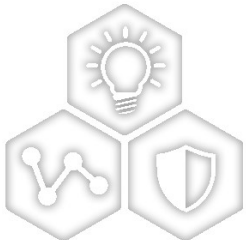


Tools to predict Single Event Effects

Soft Error Rate Estimation by Simulation



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



SMART | CONNECTED | SECURE

Aerospace and Defense
David Truyen - Technology Hardening Team

13rd December 2022

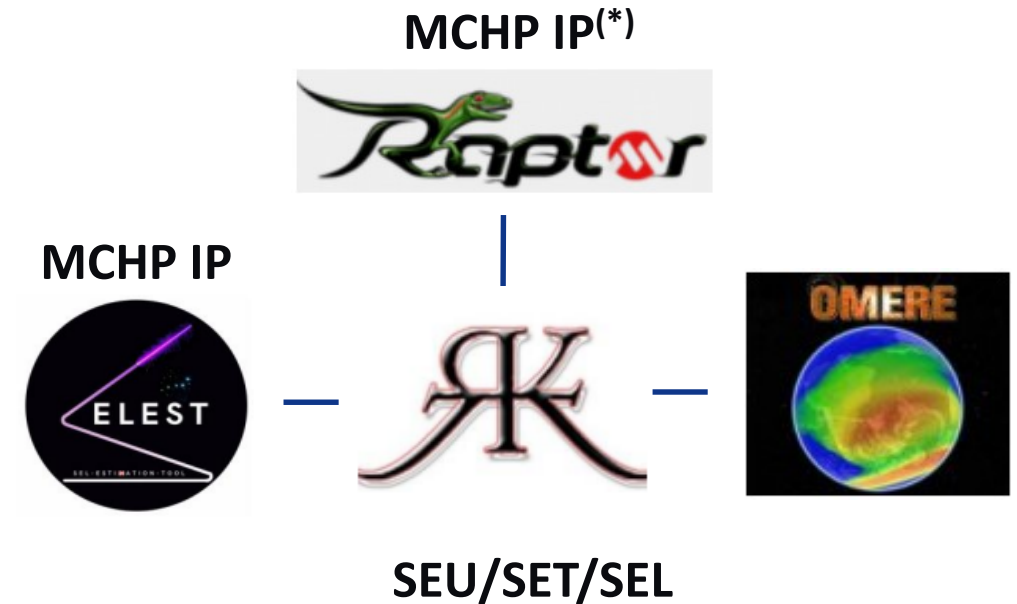
Introduction

Objectives

- **Soft & hard Errors caused by radiations is a major concern for electronic components**
- **The Technology Hardening team developed methodologies and tools to **predict the radiation sensitivity** of the products and provide **mitigation guidelines****
 - Evaluate technologies
 - Evaluate the operational risk of the cells & circuit before testing
 - Improve the reliability and efficiency of the devices (std cells)
 - Evaluate full custom IPs, clock/reset trees
 - Highlight critical parameters (process, design) and propose hardening solution

Radiation Tool Kit (RTK)

- Suite of software tool dedicated to SEL/SEU/SET radiation effects
 - TCAD 2D and 3D simulator by Synopsys
 - **RAPTOR** for SEU/SET Simulations
 - **SELEST** for SEL simulations
 - **OMERE** for SER calculation
- RTK does not address SEFI
 - Design & Application dependent
- ... and TID ?
 - Not yet available, but the feasibility of a TID predictive tool is in progress



(*) RAPTOR is a MCHP tool co-developed with the ONERA (include the code MUSCA)

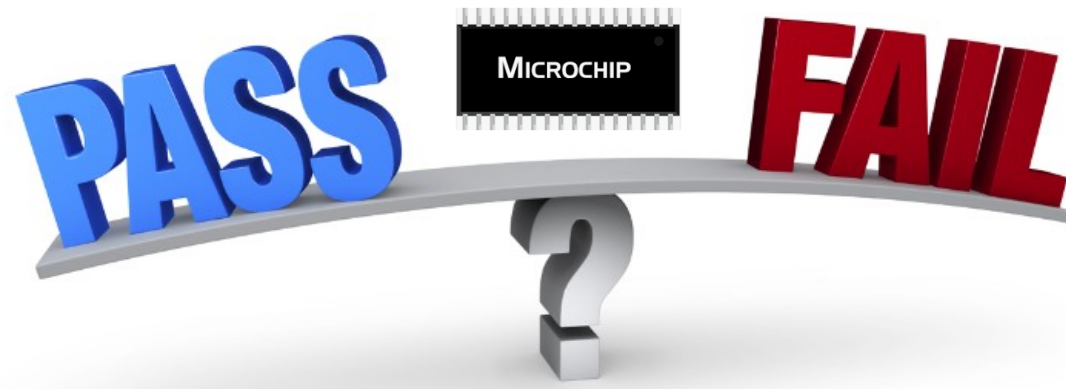
SEL Prediction by Simulation



SEL ESTimation Tool
Co-funded by the CNES

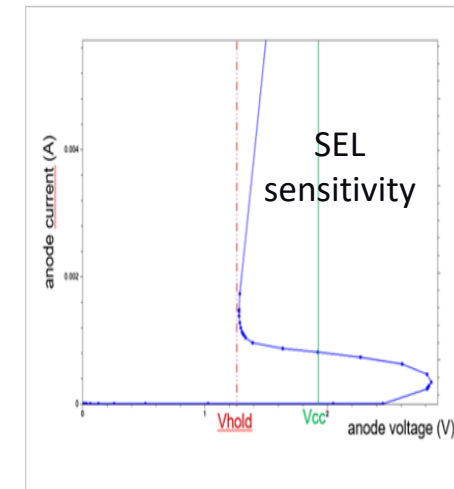
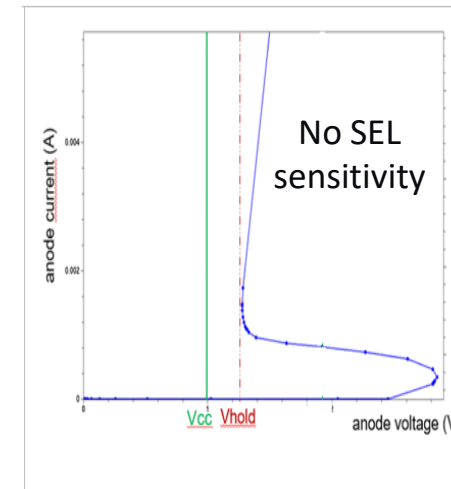
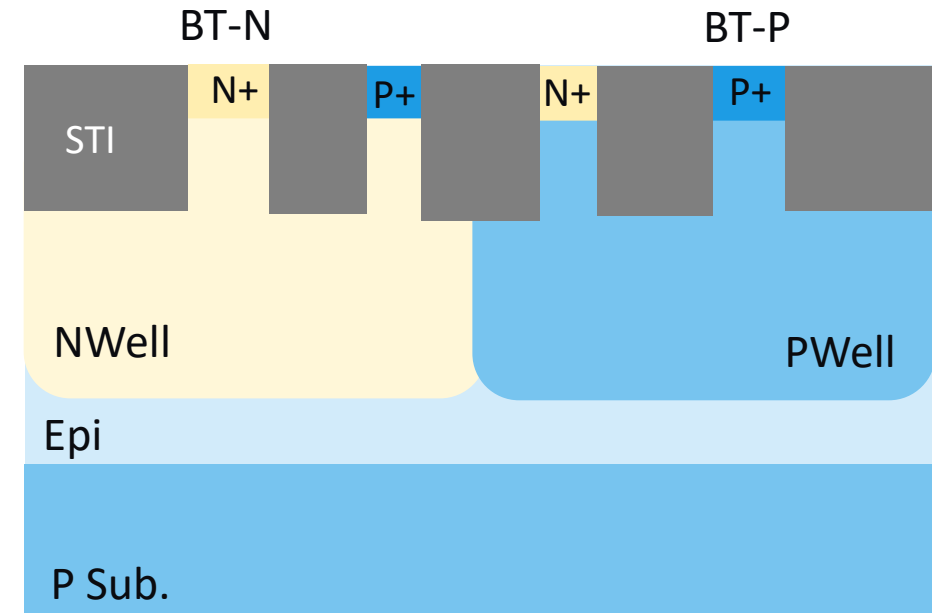
SELEST – Goal

- **Assistant tool** to select commercial components able to address the new-space market
- **Estimate the SEL sensitivity** of the products before performing tests with a tradeoff between time & accuracy
- Provide hardening solutions against SEL



SELEST – Strategy

- Define an analytical model based on TCAD simulation
- Define the SEL sensitivity by estimating the $P(V_{\text{hold}}) > V_{\text{CC}}$
- Develop analytical prediction models per technologies
- Include hardening by process parameters
- Model the effect of the temperature and power supply



Technical challenges



- **Run a huge number of simulations (> 20 000) with an acceptable time frame**
 - Run simulations by scripts instead of Interactive mode
- **Extract and analyze a huge number of TCAD results**
 - Classify the different simulation status
 - Relaunch failed simulations and update of the *output* file with new results
- **Consolidate the results**
 - Initiate dedicated TCAD studies to classify some ambiguous results
 - Check of incomplete simulations
- **Development of the model**
 - Identify the PASS-FAIL cases
 - Create a classification model by using JMP and/or Neural designer tools...
 - Optimization of the model (neural, DOE analysis, ...)
 - Include the experimental results
- **Development of a GUI interface**

Design of Experiment of TCAD Simulations

Inputs and values

- **Inputs**
 - **Process:** consider the doping profiles, resistivities, Epi, Bulk,...
 - **Topology:** consider spacings, widths, based on DRC rules of the technology
 - **Electrical:** range of the power supply Vs technology (min, max, typical)
 - **Temperature :** $85^{\circ}\text{C} \leq T \leq 125^{\circ}\text{C}$
- **Some figures about the DoE:**
 - **Number of cases:** ~20k cases per technology
 - **Duration of TCAD simulations:** 3min/simu => ~6 weeks non-stop

Analysis & Consolidation of TCAD Results

• Classification of Status

Status	Comment
LATCHUP_DETECTED	Vhold, Vtrig extracted
NO_LATCHUP	No Vhold, Vtrig (NA)
DOUBLE_S_DETECTED	Vhold, Vtrig, Vhold_reverse, Vtrig_reverse, extracted
MULTIPLE_S_DETECTED	
SDE_LICENSE_ERROR	Could not get a license. Jumped to next experiment simulation.
SNMESH_LICENSE_ERROR	
SDEVICE_LICENSE_ERROR	
NO_MESH_FILE	sde or snmesh failed
SDEVICE_FAILURE	sdevice failed (no convergence)
NO_PLOT_FILE	No plot file found
INCOMPLETE_SIMULATION	Neither max_vstress nor max_istress were reached in plot file (convergence problem)
HIGH_CURRENT_AT_VDD	High anode current at VDD
NEED_CHECK	Plot analysis found an incoherence
KO	Plot analysis could not conclude
GOT_NO_STATUS	Something went wrong in flow, but what ?

	BulkRes	DBodyTieN	DBodyTieP	Spacing_AC	STI_SAC	Temperature	Vdd	Vtrig	Vhold	Vtrig_reverse	Vhold_reverse	Status	Status_SEL
13/0 Cols	15	30	30	15	2.5	125	1.32	7.81	7.39	1.92	7.61	LATCHUP_DETECTED	0
										1.92		DOUBLE_S_DETECTED	1
										1.93		NO_LATCHUP	
										1.95		SDEVICE_FAILURE	
										1.96		INCOMPLETE_SIMULATION	
										2.241 others		MULTIPLE_S_DETECTED	
58	3	0.1	0.1	0.12	0.32	85	1	1.74	0.9			• SDEVICE_FAILURE	1
59	3	0.1	0.1	10	1	105	1					• NO_LATCHUP	1
60	3	0.1	0.1	15	1	105	1					• NO_LATCHUP	1
61	3	0.1	0.1	0.12	1	105	1.1	2.516	2.51			• LATCHUP_DETECTED	1
62	3	0.1	0.1	0.3	1	105	1.1	2.639	2.57			• LATCHUP_DETECTED	1
63	3	0.1	0.1	1	1	105	1.1	2.865	2.77			• LATCHUP_DETECTED	1
64	3	0.1	0.1	5	1	105	1.1	5.429	5.00			• LATCHUP_DETECTED	1
65	3	0.1	0.1	10	1	105	1.1					• NO_LATCHUP	1
66	3	0.1	0.1	15	1	105	1.1					• NO_LATCHUP	1
67	3	0.1	0.1	0.12	1	105	1.32	2.770	2.72			• LATCHUP_DETECTED	1

• Identification of errors

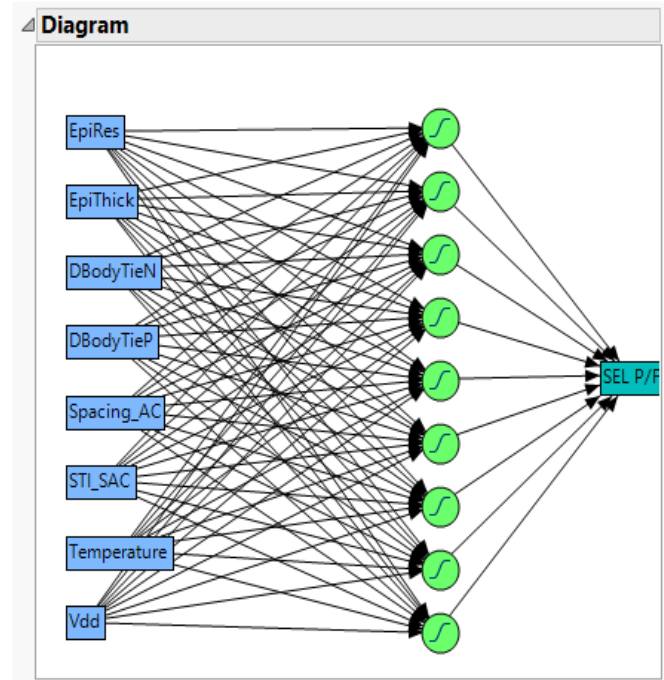
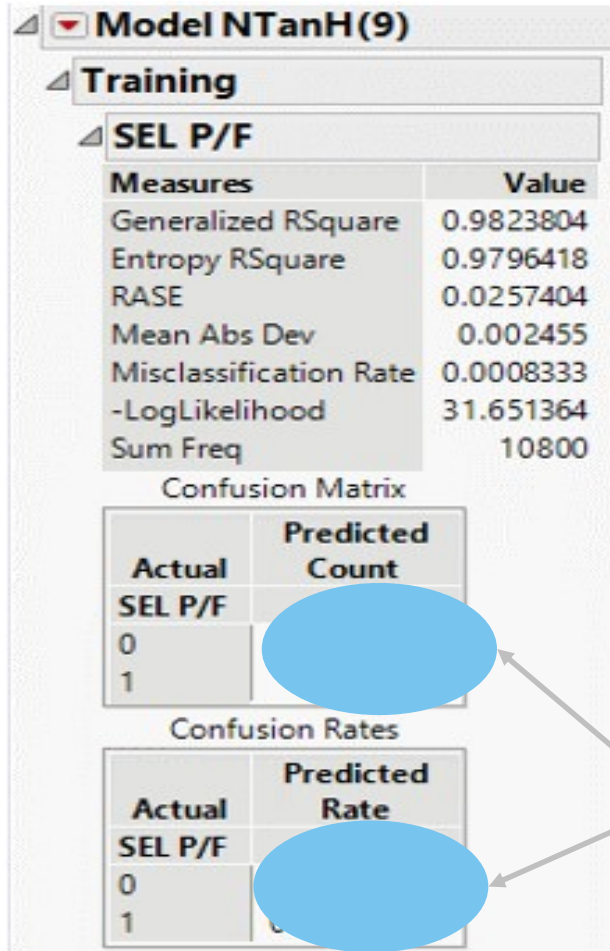
- 15 type of errors have been classified
- 900 simulations have been relaunched (convergence issues)

• Consolidation of the results

- For the 65nm technology, the full **27864** simulations have been considered to define the prediction models

Development of the Model - Epi

- Model PASS/FAIL for **EPI** process



FAIL - Latchup: $V_{\text{hold}} < V_{\text{cc}}$

PASS - No latchup: $V_{\text{hold}} > V_{\text{cc}}$

SEL : 5 erroneous predictions on 353 cases (error of 1.4%)
No SEL: 4 erroneous predictions on 10447 cases (error < 0.1%)

Validation of the Models



- **Selest Vs Experiments**

Technology	Node (nm)	Product	Manufacturer	Manuf. Location	Device	Supply (V)	Temperature (°C)	Exp LETth (MeV.cm ² /mg)	SEL Prediction by SELEST	
CMOS	65	Product 1	Manuf. 1	Fab1	SRAM	1.26	125	< 16	Model Bulk 65nm LV	SEL
CMOS	65	Product 2	Manuf. 1	Fab1	SRAM	1.26	125	< 16		SEL
CMOS	65	Product 3	Manuf. 1	Fab1	Std cells	1.26	125	> 65		No SEL
CMOS	65	Product 4	Manuf. 1	Fab1	Std cells	1.40	125	> 62		no SEL
CMOS	65	Product 5	Manuf. 1	Fab1	Std cells	1.30	125	> 62		No SEL
CMOS	65	Product 6	Manuf. 1	Fab1	SRAM	1.00	125	> 62		No SEL
CMOS	65	Product 7	Manuf. 2	Fab2	SRAM	1.32	125	TBD		SEL
CMOS	65	Product 7	Manuf. 2	Fab2	Std cells	1.32	125	TBD		SEL

Good correlation between Estimations and experiments

Criteria: $LET_{th} > 60 \text{ MeV.cm}^2/\text{mg} \rightarrow \text{No SEL}$

Pending experimental results of 65nm Epi process

Development of a Graphical Interface



SELEST v1.0.3

SEL Evaluation PASS / FAIL

Open Save Save As... About

Models

Interactive

DRC Matrix

Data Source

Variables

Variable name	Value
BulkRes	10
DBodyTieN	29
DBodyTieP	29
STI_SAC	0.3
Spacing_AC	0.29
Temperature	125
Vdd	1.32

Std cells, worstcase

Models result

Model	Model Output	Use
65nm Bulk Proba (No SEL) in %	0.0	Bull

SEL

Models Interactive **DRC Matrix** Data Source

SEL Mitigations

Matrix Parameters

Model 65nm Epi LV - Pr Model Output Threshold 50 Z display Min

min 0.1 max 5 Lin. samples 50

min 0.1 max 5 Lin. samples 50

min 0.1 max 5 Lin. samples 50

Variable name

Value

Compute Matrix

Export Matrix

EpiThick 3

STI_SAC 0.4

Spacing_AC 0.5

Temperature 125

DBodyTieN

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
2	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2
4	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
5	1.3	1.3	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
6	1.3	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.1
7	1.3	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1
8	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1
9	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
10	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
11	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
12	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
13	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
14	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
15	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
16	1.3	1.3	1.3	1.2	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
17	1.3	1.3	1.3	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
18	1.3	1.3	1.3	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
19	1.3	1.3	1.3	1.2	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
20	1.3	1.3	1.3	1.2	1.2	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1

DBodyTieP

Vdd

DBodyTieP

DBodyTieN

Example of Mitigation : Voltage derating Vs distance of body-ties

Thank you for your attention

Questions ??

BACKUP



Aerospace &
Defense Group



Prospects

- **Development of next models :**

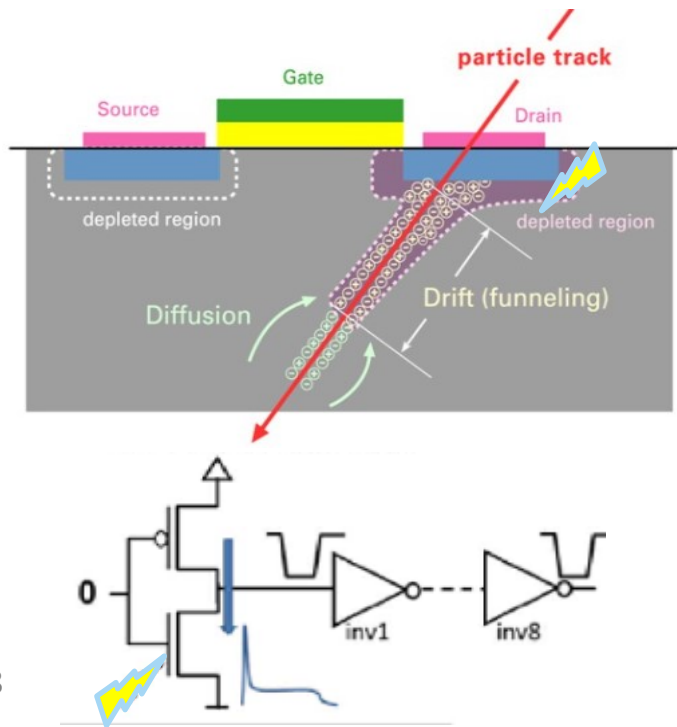
- 180nm
- 150nm SOI
- 130nm
- 110 nm (in progress)
- 90nm
- 28nm
- 12nm FinFet

Single Event Effects

- SEE are radiation induced errors due to a *single particle* (protons, heavy ions, neutrons, Alpha)

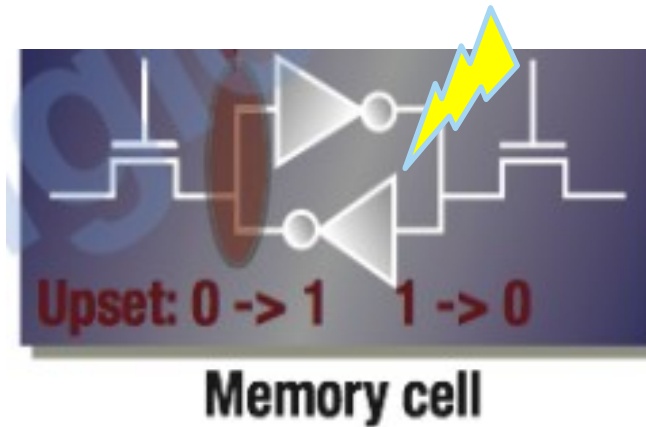
Single Event Transient

SET is a current pulse occurring at a circuit node



Single Event Upset

SEU is a change of state of memory cell



SEL is an abnormal high-current state in a device
=> May cause permanent damage to the device

